A Low-Power and High-Performance CMOS Fingerprint Sensing and Encoding Architecture

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***Abstract*— A CMOS fingerprint sensor architecture with embedded cellular logic for image processing is presented. The system senses a fingerprint image with a capacitive technique and performs several image-processing algorithms, including thinning the ridges of the fingerprint structure and encoding it to its characteristic features. Image processing is achieved by application of hexagonal local operators implemented in pixel-parallel mixed neuron-MOS/CMOS logic circuits. The massive parallelism of the architecture leads to a very low power dissipation. Results of simulations and measurements on a demonstrator chip in 0.65-μm double-poly standard CMOS technology are shown. The approach is well suited for person-identification applications, especially in small and low-cost portable systems, such as smart cards.**

***Index Terms*— Cellular automaton, fingerprint encoding, fingerprint sensor, image processing, low-power design, neuron MOS, pixel-parallel circuits.**

I. Introduction

A SYSTEM for automatic fingerprint recognition consists of three components: a sensing unit for acquisition of the fingerprint image, an encoding unit for extraction of the characteristic features of this image, and a matching unit for comparison of the extracted feature set with a certain stored feature set. For low-cost applications, sensing units based on capacitive sensors in CMOS and thin-film-transistor technologies have been presented [1]–[3]. However, for the encoding unit, no suitable architectures for this class of applications have been presented so far, as this stage of processing is computationally expensive. Commonly, the irregularities of the ridge structure of the fingerprint image are examined and used as features to encode the image [4]–[6]. These so-called minutiae are basically the ending and bifurcation points of the ridges. Having located the relative positions of these characteristic feature points, the obtained set of points is compared with reference sets in a data base by standard pattern-matching techniques.

In this paper, we present a CMOS fingerprint sensor architecture which combines sensing and encoding capabilities in a single-chip system with low power consumption and low area requirements [7]. Studies have shown that in fingerprint identification algorithms, over 90% of computational power has to be spent on image processing and minutiae extraction, the remaining 10% on pattern matching. Similar results can also be found in [6]. For this reason, pattern matching is not considered here. Fig. 1 depicts the processing steps implemented in our architecture for sensing and encoding a typical fingerprint image. First, the input image is acquired by an array of capacitive sensor elements. Then, the locations of the ridge endings can be obtained by thinning the binary input image to one-pixel-wide lines and localizing the ending points and bifurcations.

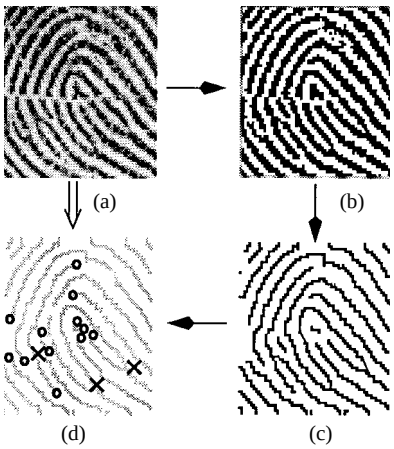

Fig. 1. Processing steps from (a) the sensed fingerprint image to (d) the extracted minutiae (○: ridge endings, ×: ridge bifurcations). (a) Image acquisition, (b) binarization, (c) thinning, and (d) minutiae extraction.

Local morphological operators are well suited for such image-processing tasks. These operators can be implemented directly and efficiently in a massively parallel cellular architecture with locally connected identical processing units (PU's) which are embedded into a sensor array (see [8]–[10]). For the analysis of fingerprint images certain local operators have been proposed. A hexagonal arrangement of the pixels has been proven to be particularly advantageous for fingerprint images [11], [12]. Unlike in rectangular grids, in hexagonal grids two adjacent pixels always have the same distance from each other (there are no diagonal neighbors). This property leads to simple formulations of morphological operators and thus to a less complex circuit design. The built-in algorithms include removal of single white pixels in a black object, elimination of single black pixels on the edge of black objects, thinning of black objects to one-pixel-wide lines, and, finally, extraction of the ridge endings from the thinned image. The bifurcations of the ridges can be obtained by extraction of the ridge endings of the inverted image in a second processing pass. The extraction of the minutiae from the input image can be regarded as data reduction on a sensor level.

Manuscript received November 4, 1998; revised January 21, 1999. This work was supported by an Ernst von Siemens Scholarship.

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Publisher Item Identifier S 0018-9200(99)04727-7.

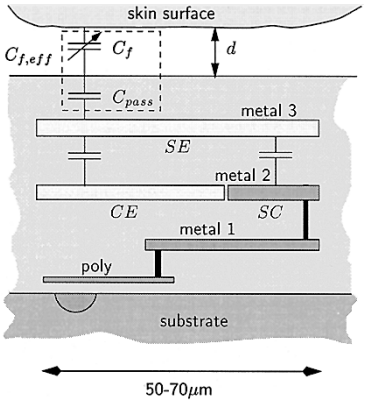

Fig. 2. Schematic cross section of a PU with the relevant parasitic capacitances of the sensor electrode. The circuits of the PU are wired with metal 1 and poly.

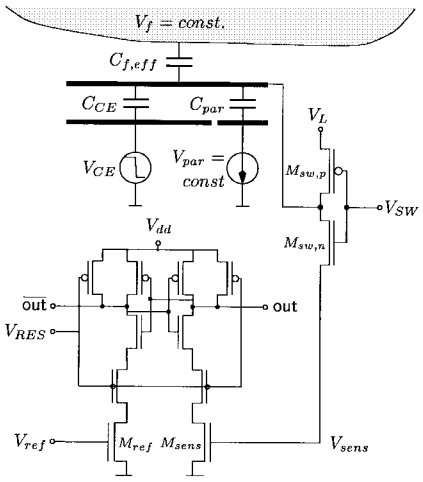

Fig. 3. Sensor circuit with dynamic latch as comparator for binarization of image data.

Massive parallelism in CMOS circuits has a positive effect on the power dissipation [13]. As each pixel has its own processing circuit distributing the computation over the array, the clock rates can be chosen very low, enabling us to design slow circuits with low dynamic energy dissipation or to apply low-voltage techniques. Furthermore, the inherent tolerance to technology-related defects (redundancy) and low wiring complexity (cellularity) contribute to a robust and energy-efficient design of parallel circuit architectures. The proposed sensor array is thus applicable for low-power portable systems, such as smart cards. As the image-processing circuitry is fully embedded into the sensor array, no additional area is required.

This paper is organized as follows. Section II describes the applied capacitive sensing technique and the implementation concept in a standard CMOS technology. Then, the implementation of image-processing algorithms in cellular pixel-parallel PU's and the encoding procedure are presented. Measured results on a demonstrator chip fabricated in a 0.65-μm technology are shown and discussed in Section III. Experimental results on the power dissipation and the functionality of the chip are presented. Section IV concludes this paper.

II. Circuitry of the Cellular Array

A. Capacitive Sensing Scheme

In Fig. 2, the cross section of a sensing and processing unit is shown. For the acquisition of the fingerprint image, a capacitive sensing technique is applied. We evaluate the effective capacitance $C_{f,\mathrm{eff}}$ between the skin of the finger and a top metal electrode plate for each pixel. Below the sensor electrode (metal 3), global supply and control lines *SC* and a coupling electrode *CE* are designed in metal 2. The circuits of the pixel-parallel processing logic are placed directly below the sensor electrode and are wired with metal 1 and poly-silicon.

Fig. 3 depicts the sensing and coupling electrode with the respective voltage sources. After the finger is placed on the surface of the chip, the sensor electrode is first charged to $V_{\mathrm{sens}} = V_L$ via $M_{\mathrm{sw},p}$ with the switching signal $V_{\mathrm{SW}} = \mathsf{lo}$. The amount of electric charge on the electrode is directly dependent on $C_{f,\mathrm{eff}}$ and, hence, on the distance d of the skin to the electrode. Then, after switching $V_{\mathrm{SW}} = \mathsf{hi}$, also the potential of the coupling electrode V_{CE} is lowered by an amount of ΔV_{CE}, leading to the potential of the floating sensor electrode

$$V_{\mathrm{sens}} = V_L - \Delta V_{\mathrm{CE}} \cdot \frac{1}{1 + \frac{C_{\mathrm{par}}}{C_{\mathrm{CE}}} + \frac{C_{f,\mathrm{eff}}}{C_{\mathrm{CE}}}}. \quad (1)$$

C_{CE} and C_{par} are the capacitances between sensor electrode and coupling electrode and between sensor electrode and supply and control lines, respectively. Both the potential of the finger and of the supply and control voltages can be chosen arbitrarily but have to be constant during the sensing process.

The maximum voltage swing ΔV_{sens} is the difference between $V_{\mathrm{sens}}(C_{f,\mathrm{eff,max}})$ and $V_{\mathrm{sens}}(C_{f,\mathrm{eff,min}})$. For $C_{f,\mathrm{eff,min}} = 0$ fF, this voltage swing results in

$$\Delta V_{\mathrm{sens}} = \Delta V_{\mathrm{CE}} \cdot \frac{C_{f,\mathrm{eff,max}}}{\left(1 + \frac{C_{\mathrm{par}}}{C_{\mathrm{CE}}}\right)\left(1 + \frac{C_{\mathrm{par}}}{C_{\mathrm{CE}}} + \frac{C_{f,\mathrm{eff,max}}}{C_{\mathrm{CE}}}\right)}. \quad (2)$$

In the demonstrator circuit, we have to consider additional junction capacitances of the switching transistors and losses of electrode charge due to leakage currents. This leads to slightly different values for V_{sens} in circuit simulations compared to (2). For typical values ($V_L = 5$ V, $\Delta V_{\mathrm{CE}} = 5$ V, $C_{\mathrm{CE}} = 105$ fF, $C_{\mathrm{par}} = 121$ fF), and $C_{f,\mathrm{eff,max}} = 60$ fF, (2) predicts a voltage swing of $\Delta V_{\mathrm{sens}} = 487$ mV, whereas simulated results shown in Fig. 4 lead to $\Delta V_{\mathrm{sens}} = 379$ mV.

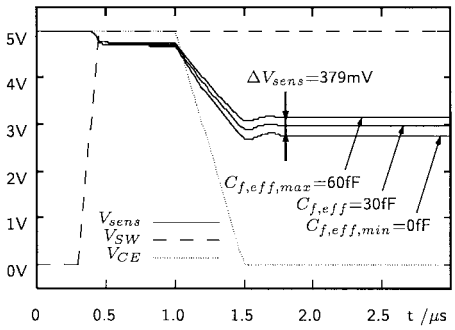

Fig. 4. Simulated $V_{\mathrm{sens}}(t)$ with $C_{f,\mathrm{eff}}$ as parameter ($V_L = 5$ V, $\Delta V_{\mathrm{CE}} = 5$ V, $C_{\mathrm{CE}} = 105$ fF, $C_{\mathrm{par}} = 121$ fF).

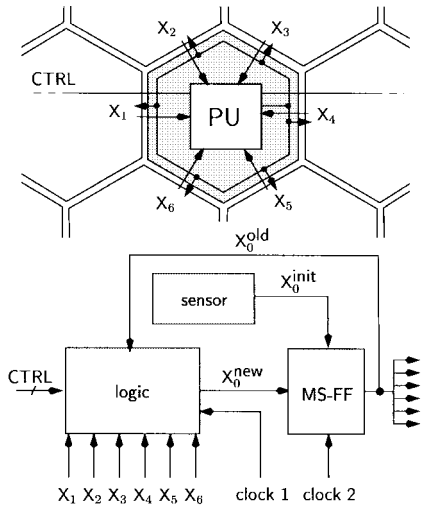

Fig. 5. Basic structure and input–output configuration of a PU with its six neighbors.

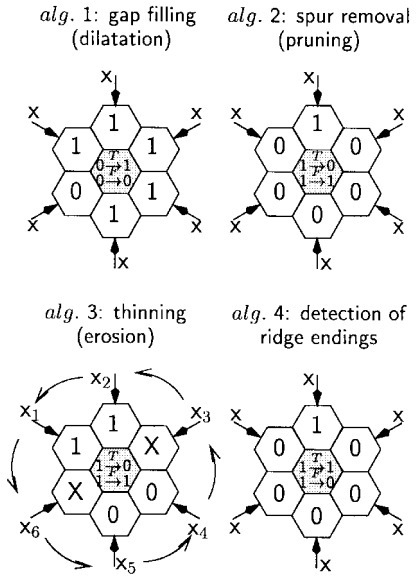

Fig. 6. Implemented structuring elements with boolean conditions for binary morphological image processing (T: true; F: false).

To convert the obtained signal into a binary value, V_{sens} and a reference potential V_{ref} are connected to the input transistors M_{sens} and M_{ref} of a comparator stage, respectively. The comparator stage is implemented as a dynamic latch comparator, as presented in [14] and [15], which compares the conductances of its two input transistors (see Fig. 3). When the trigger signal V_{RES} is changed from lo to hi, the latch is in a metastable state with $OUT = \overline{OUT} =$ hi. With the rising slope of V_{RES}, one of the two output nodes is discharged to lo, depending on the input voltages V_{sens} and V_{ref}. After evaluation, the result is latched as binary value in each pixel element. Since high-speed operation of the comparator circuit is not required here, the circuit can be optimized for high resolution. For this reason, the transistor sizes are chosen relatively large ($20 \times \text{area}_{\min}$) to ensure a sufficient matching behavior and low offset-voltage deviations across the sensor array.

In this approach, V_{ref} is supplied from an off-chip source. To obtain images of good quality, this voltage has to be attuned to a value corresponding to an average level of V_{sens} of the whole sensor array. A technique for automatic local adaptation of V_{ref} is a subject of current work.

B. Configurable Sensing and Processing Unit

After the input image of the fingerprint structure has been acquired, local morphological operators process the binary image data. Several distinct image-processing algorithms are necessary for encoding, which have to be implemented into each PU. Each PU can be configured via control lines by an external control logic to perform a certain image-processing step.

The basic structure of each PU consists of a logic block, a status register, and a sensor circuit (see Fig. 5). In the first step, the register is initialized by the sensing process. Within each subsequent clock cycle, the logic block first computes a new pixel value depending on the old value of the PU X_0^{old} and the old values of the six neighboring PU's $X_{1,\ldots,6}$ (clock 1). Then, the new result X_0^{new} is shifted into the status register (clock 2) so that it is available for the evaluation in the next clock cycle. All PU's are clocked synchronously and in parallel. The logic block is configured by the CTRL lines. Architectures like this with many identical processing elements with local connections are called *cellular automata*.

Fig. 6 depicts the templates and the boolean conditions for the value of the central pixel for the four implemented morphological operators. These algorithms can be directly formulated in threshold logic terms combined with boolean conditions as in

$$\text{if } X_0^{\text{old}} = a \quad \text{and} \quad \sum_{j=1}^{6} w_j \cdot X_j > \Theta, \quad \text{then } X_0^{\text{new}} = \bar{a} \quad \text{else } X_0^{\text{new}} = a \tag{3}$$

with a representing the state of the PU X_0, w_j the weighting factors for each of the six neighboring inputs X_j, and Θ a threshold value. Threshold equations can be advantageously implemented with neuron MOS transistors [16]. A neuron MOS transistor is a floating-gate transistor with several coupling gates. The w_j correspond to the sizes of the coupling gates and the resulting floating-gate potential is a weighted sum of the input voltages of the coupling gates. Details on the design of such threshold logic gates and examples for other implementations can be found in [17] and [18].

The logic block is implemented using a dynamic latch comparator with two neuron MOS transistors as input transistors completed by additional logic gates. Fig. 7 shows the circuit with an example threshold equation and Fig. 8 the block diagram of the complete PU. The application of neuron MOS circuitry leads to a reduced gate complexity and, thus, to low-power design on circuit level. The combination of boolean and threshold logic avoids the presence of disadvantageous huge input weights in the threshold equations. Similar to the sensing scheme (see Section II-A), here the conductances of the two neuron MOS transistors have to be compared in order to compute the threshold logic equations. To execute

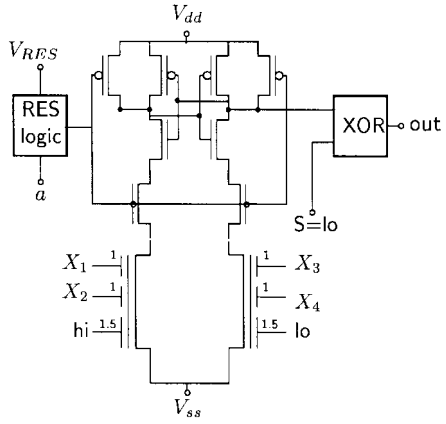

Fig. 7. Structure of the implemented logic block with neuron MOS threshold gate and additional boolean logic gates. In this example, the threshold function $X_1 + X_2 > X_3 + X_4 + 1.5$ is shown.

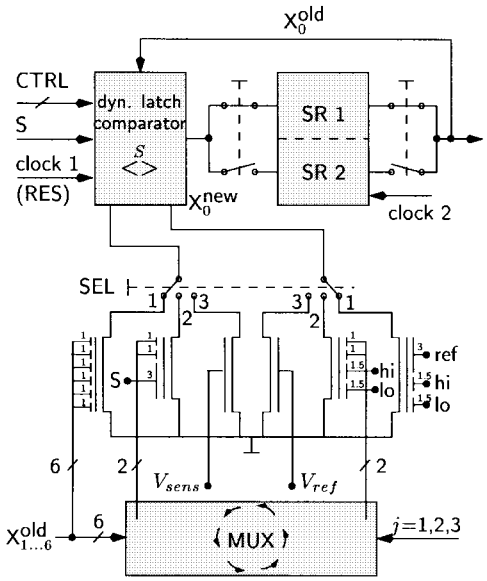

Fig. 8. Block diagram of the configurable PU (SEL = 1: Algorithms 1, 2, and 4; SEL = 2: Algorithm 3; SEL = 3: sensing process).

both comparisons with one comparator circuit, the dynamic latch from Fig. 3 is completed with an additional enable logic controlling $V_{\rm RES}$. If condition $X_0 = a$ is not fulfilled, the RES signal is not applied to the latch and the comparison is not performed. Furthermore, the input transistors of the latch can be selected to be either a neuron MOS transistor pair or the transistor pair with $V_{\rm sens}$ and $V_{\rm ref}$ as gate voltages. This selection is accomplished by a NMOS pass transistor tree represented by switch *SEL* in Fig. 8. The signal S and the XOR circuit determine whether to perform a "greater than" or a "less than" comparison by choosing either *OUT* or $\overline{OUT}$ as the output of the comparator. This is indicated by $\overset{S}{<>}$, which denotes $<$ for $S = 0$ and $>$ for $S = 1$, respectively. This comparator stage is the basic circuit for the configurable sensing and processing unit.

The algorithms for removal of single white pixels (Algorithm 1), elimination of single black pixels or spurs (Algorithm 2), and extraction of the ridge endings from the thinned image (Algorithm 4) simply execute a comparison of the sum of the six neighboring values ΣX_i with a threshold value (*SEL* $= 1$ in Fig. 8). For example, in Algorithm 1, a pixel is set if the sum of its six neighbors is equal or greater than five. Thus, all white pixels surrounded by at least five black ones become black in the next clock cycle. The logic conditions with their corresponding threshold equations for these algorithms with $w_j = 1$ and $\Theta = 1.5 + 3 \cdot \mathsf{ref}$ are expressed in (4) at the bottom of the page.

If either the condition for $X_0^{\rm old}$ or the comparison is not true, the pixel remains unchanged. Note that Algorithms 2 and 4 differ in the conclusion only. The boolean conditions are realized with the above-mentioned enable logic, which controls the signal $V_{\rm res}$ of the comparator. For example, in Algorithm 1, the threshold equation will be computed (i.e., the RES input of the comparator is activated) only if $X_0^{\rm old} = 0$. Otherwise, the value stored in the comparator remains unchanged. This strategy also contributes to power saving, as for a great number of the pixels the condition is not true and the comparison is not performed (for Algorithm 1, the condition is true for all black pixels only, which is approximately half the number of total pixels in a homogeneous input image).

The algorithm for thinning black objects to one-pixel-wide lines (Algorithm 3) decides iteratively whether to erase black pixels that belong to the edge of an object, until the object's one-pixel-wide skeleton remains [11]. Each pixel is regarded as a border pixel; if two adjacent neighboring pixels are "black," the opposite ones "white," and the remaining pixel values "don't care." Due to the symmetry of the hexagonal grid, this template can be applied six times, rotated 60° successively. We formulated this thinning algorithm in an elegant manner with a single threshold equation (*SEL* $= 2$ in Fig. 8). The algorithm runs at six clock cycles, where two opposite pairs of inputs are switched successively to the logic block by means of the multiplexers MUX, consisting of complementary transfer switches.

Fig. 9 shows the truth table for $X_0^{\rm old}$ of the thinning algorithm. The four inputs of this logic function are denoted as $X_{(j)}$, $X_{(j+1)}$, $X_{(j+3)}$, and $X_{(j+4)}$, where $X_{(k)}$ means $X_{k \bmod 6}$ and j describes the multiplexer MUX for cyclic shift of the inputs. For each given input configuration $(j = 1, 2, 3)$, two successive evaluations with $S = 0$ and $S = 1$ are performed

$$\begin{aligned} &S = 0\text{: } X_{(j)} + X_{(j+1)} + \bar{X}_{(j+3)} + \bar{X}_{(j+4)} < 0.5 \\ &S = 1\text{: } X_{(j)} + X_{(j+1)} + \bar{X}_{(j+3)} + \bar{X}_{(j+4)} > 3.5. \end{aligned} \quad (5)$$

$$\begin{aligned} &(\text{Algorithm 1}) \quad \text{if } X_0^{\rm old} = 0 \quad \text{and} \quad \Sigma X_i > 4.5, \quad \text{then } X_0^{\rm new} = 1 \\ &(\text{Algorithm 2}) \quad \text{if } X_0^{\rm old} = 1 \quad \text{and} \quad \Sigma X_i < 1.5, \quad \text{then } X_0^{\rm new} = 0 \\ &(\text{Algorithm 4}) \quad \text{if } X_0^{\rm old} = 1 \quad \text{and} \quad \Sigma X_i > 1.5, \quad \text{then } X_0^{\rm new} = 0 \end{aligned} \quad (4)$$

X		$\overline{X}$		$\sum$	X_0^{new}	
(j)	$(j+1)$	$(j+3)$	$(j+4)$		$S=0$	$S=1$
0	0	0	0	0	1	0
0	0	0	1	1	1	1
0	0	1	0	1	1	1
0	0	1	1	2	1	1
0	1	0	0	1	1	1
0	1	0	1	2	1	1
0	1	1	0	2	1	1
0	1	1	1	3	1	1
1	0	0	0	1	1	1
1	0	0	1	2	1	1
1	0	1	0	2	1	1
1	0	1	1	3	1	1
1	1	0	0	2	1	1
1	1	0	1	3	1	1
1	1	1	0	3	1	1
1	1	1	1	4	0	1

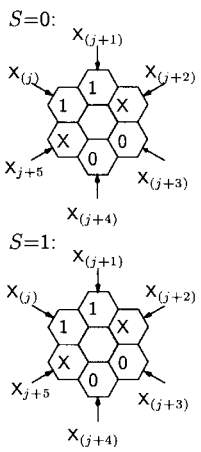

Fig. 9. Truth table for X_0^{new} in Algorithm 3. With $j = 1, 2, 3$ and $S = 0, 1$, all six subcycles of the thinning algorithm can be realized.

The two resulting threshold equations in (5) can be formulated as a single one using S as auxiliary input value. If $X_0^{\mathrm{old}} = 1$ and

$$X_{(j)} + X_{(j+1)} \overset{S}{<>} X_{(j+3)} + X_{(j+4)} + 3 \cdot S - 1.5 \qquad (6)$$

then $X_0^{\mathrm{new}} = 0$. In (6), the signal S determines both the polarity and the threshold value of the comparison. Thus, a linearly nonseparable function can be expressed with a single threshold equation. Together with parameter j, (6) has six different states, which correspond to the above-mentioned six clock cycles. This algorithm has to be applied to the image several times, depending on the ridge width of a typical fingerprint structure. After each execution, Algorithm 2 has to be applied in order to eliminate one-pixel-wide extensions of black objects. Otherwise, these extensions would result in spurious branches and ridge endings, diminishing the quality of the encoding result.

C. Encoding Procedure

In Section II-B, the implementation of several image-processing algorithms was described. These algorithms have to be applied to the input image several times in a distinct order.

Directly after image sensing, Algorithms 1 and 2 are repeated several times to eliminate noise in the input image. Then, Algorithm 3 (with all six subcycles) and Algorithm 2 are applied several times to reduce the ridge image to its one-pixel-wide skeleton. Last, Algorithm 4 deletes all black pixels with exception of the ending pixels. This information is then read out of the array and used for point-pattern matching.

Algorithms for extracting bifurcations of ridge endings are not implemented directly. As the bifurcations of black ridges are nothing but the endings of the white ridges, they can be regarded as the endings of the inverted image. For this reason, each PU contains an additional second status register SR 2, in which the inverted image is stored after the sensing process. After the ridge endings of the image are extracted and read out, the inverted image is invoked, and the complete procedure is repeated.

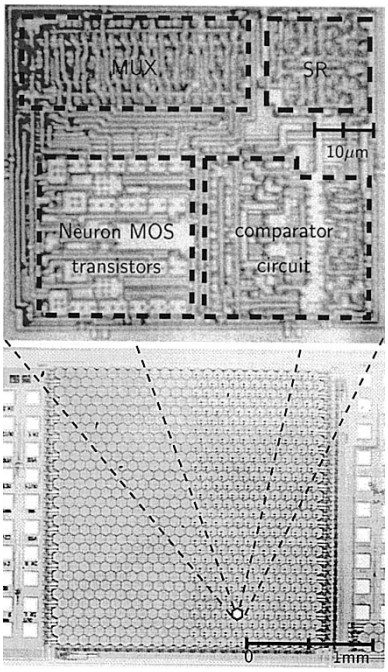

Fig. 10. Photograph of (a) a PU hidden below each hexagonal sensor electrode and (b) the demonstrator circuit.

D. Composition of the Array Structure

The described PU's are arranged in a completely regular manner on a hexagonal grid. For readout of the state of the array, all outputs of the PU's are connected via column and line transistors to a common output line. Each PU can be selected with an addressing circuit located at the edge of the array. With this additional circuitry, the state of the array can be read out in a serial manner for testing purposes after any processing step.

III. Results and Discussion

A demonstrator chip with a 25×30 pixel sensor array was realized in a 0.65-μm CMOS double-poly three-metal-layer process. This leads to a sensor area of approximately 2×2 mm^2. Each of the 750 PU's contains 119 usual MOSFET's and four neuron MOS transistors. With the technology used, the size of a single PU is 71.4×82.5 μm^2, which corresponds to an effective lateral image resolution of approximately 330 dpi. In Fig. 10, chip photographs of the array and of a single PU are shown.

The power dissipation of the sensing and processing array on the demonstrator chip has been measured and simulated at different supply voltages. The results are shown in Fig. 11, where all values are scaled from 750 PU's to a full-size sensor array with 40 000 PU's. Note that the power dissipation depends on the input image and has a lower and an upper bound. Running at a very low clock rate of 5 kHz, a full-sized sensor array is expected to dissipate less than 6.7 mW at 5 V and with a reduced supply voltage of 2.5 V only 0.25 mW. Note that only the circuits of the PU itself are considered here, excluding the generation of the control signals. The relatively large peak current in a full-size array occurring at the transients of the clock signals is presently under investigation.

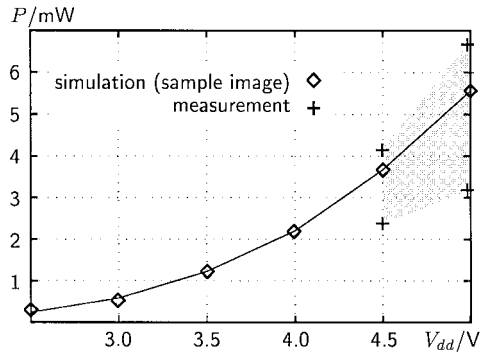

Fig. 11. Simulated and measured power dissipation at different supply voltages at a clock rate of 5 kHz (scaled to 40 000 PU's). Peripheral circuits are not considered.

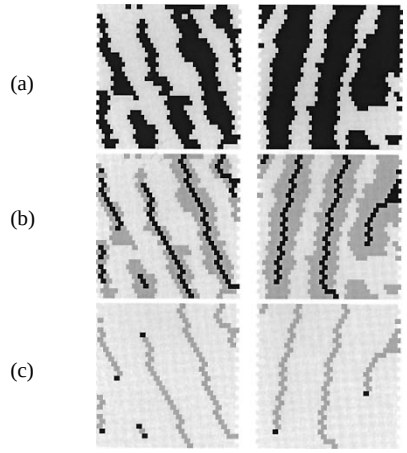

Fig. 12. Two typical measurement results: (a) sensed images, (b) their skeletons, and (c) the extracted ridge endings. In each image, the previous one is highlighted as a gray shadow.

TABLE I
ELECTRICAL AND ARCHITECTURAL FEATURES

	(values scaled to 40,000 PUs)
power dissipation	0.25 – 6.7mW
supply voltage	2.5 – 5.0V
clock rate	5kHz
encoding time	< 20ms
transistor count	4,920,000
image resolution	330dpi

If it exceeds a critical limit for certain applications, it can be reduced by clocking the array row by row instead of in parallel.

As the processing of a fingerprint image takes 80–100 parallel clock cycles, the complete acquisition and encoding of a fingerprint image can be done in less than 20 ms at a clock rate of 5 kHz. In Fig. 12, two experimentally obtained sample images, the corresponding thinned images, and finally the extracted ridge endings are shown. These results prove the functionality of the array architecture and the feasibility of the concept in a standard CMOS process.

Table I summarizes some important electrical and architectural features of a full-size array. Preliminary examinations of an optimized circuit indicate a further reduction of power dissipation by 30%.

IV. CONCLUSION

A massively parallel sensor and processor architecture for both acquisition and encoding of fingerprint images has been presented. The feasibility of this architecture in a standard double-poly CMOS process has been shown experimentally with a demonstrator chip. Due to the massive parallelism and the application of neuron MOS circuitry, a low-power design on both system and circuit level is achieved. No additional chip area for image-encoding circuitry is needed.

In contactless smart cards, the fingerprint sensor, encoder, and matcher should preferably be implemented on a single chip. As the approach presented here offers both low-power dissipation and sensor-embedded logic, it is relevant for low-cost person-identification systems.

ACKNOWLEDGMENT

The authors would like to express special thanks to their colleague and friend A. Luck, who died unexpectedly in September 1998. With his fundamental knowledge of neuron MOS circuitry, he helped them in many discussions to recognize and solve technology- and circuitry-related problems. They also would like to thank W. Jacobs for support in simulation techniques, H. Mulatz for packaging of the demonstrator chip, and C. Pacha for early conceptual discussions.

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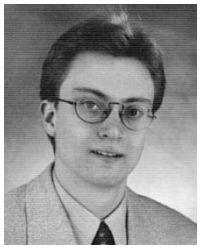

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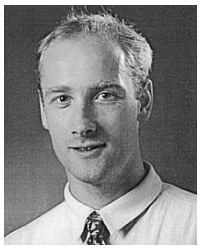

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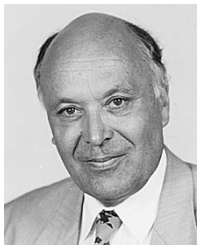

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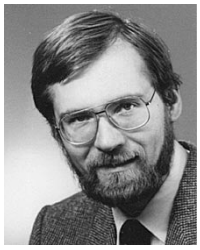

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